

Amendment of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A manufacturing method of a semiconductor IC device, comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening;

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

and using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate to form connecting holes.

2. (currently amended) A manufacturing method of a semiconductor IC device comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening;

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate to form an opening on the insulating film, followed by the formation of separating trenches on the semiconductor substrate or SOI substrate exposed from the opening;

burying an insulating film in the separating trenches to form a separating portion.

3. (currently amended) A manufacturing method of a semiconductor IC device comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening;

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

and using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate to form wiring-forming trenches on the insulating film, followed by burying an electroconductive material in the wiring-forming trenches to form a wiring layer made of the electroconductive material.

4. (previously amended) The manufacturing method described in Claim 1, wherein the insulating film is selected from the group consisting of a silica film, SOG film, PSG film, BPSG film, or a lamination consisting of these films, the first mask film and second mask film for the hook-shaped hard mask being selected from the group consisting of a polysilicon film, tungsten film, or other electroconductive film, or a silicon nitride film or other insulating film.

5. (previously amended) The manufacturing method of a semiconductor IC device described in Claim 1, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.

6. (previously presented) The manufacturing method of a semiconductor IC device described in Claim 4, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.

7. (previously presented) The manufacturing method described in Claim 2, wherein the insulating film is selected from the group consisting of a silica film, SOG film, PSG film, BPSG film, or a lamination consisting of these films, the first mask film and second mask film for hook-shaped hard mask being selected from the group consisting of a polysilicon film, tungsten film, or other electroconductive film, or a silicon nitride film or other insulating film.

8. (previously presented) The manufacturing method of a semiconductor IC device described in Claim 7, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.

9. (previously presented) The manufacturing method described in Claim 3, wherein the insulating film is selected from the group consisting of a silica film, SOG film, PSG film, BPSG film, or a lamination consisting of these films, the first mask film and second mask film for hook-shaped hard mask being selected from the group consisting of a polysilicon film, tungsten film, or other electroconductive film, or a silicon nitride film or other insulating film.

10. (previously presented) The manufacturing method of a semiconductor IC device described in Claim 9, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.